REMARKS

This response is submitted in response to the Examiner's Action dated October 19, 2005. The response answers and overcomes all rejections by the Examiner. Applicant respectfully requests that the Examiner issue a notice of allowance for all pending claims.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

I. Applicant's claimed invention is not rendered obvious because the suggested combination does not teach or suggest all of the elements of Applicant's claims.

At page 2 of the present Office Action, Claims 1, 15 and 22 are rejected under 35 U.S.C. 103(a) as being rendered obvious by U.S. Patent No. 6,393,587 to Bucher, *et al.* (*Bucher*) in view of U.S. Patent No. 6,389,000 to Jou (*Jou*). Applicants respectfully submit that exemplary Claim 1 is not rendered obvious by the combination of *Bucher* with *Jou*, because that combination does not teach or suggest all of the elements of Applicant's claimed invention, as recited in exemplary Claim 1. Specifically, with respect to exemplary Claim 1, the Examiner asserts:

> Bucher discloses a communication device, computer program product, and method for transferring data between two devices coupled to a network, said communication device comprising...a plurality of low speed interfaces, each connected to a respective one of a plurality of links to said second device, for transmitting data from said dual-port memory to said respective one of said plurality of links at one of a plurality of data rates, wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible (column 9, lines 11-35).

Applicant respectfully traverse's the Examiner's assertion that *Bucher* either teaches or suggests "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible," as recited in Applicant's exemplary claim 1. The cited text discloses

> Referring now to **FIG. 7**, a logic chart depicting a data transfer process is shown. Specifically, the transfer process is initiated under logic step **70** by setting DRAM address counter **18** to starting address of data transfer. Subsequently, terminal address register is set to ending address data transfer under logic step **72**. Thereafter, the logic proceeds to set for data transfer from DRAM to low speed host processor port **28** under logic step **74**. Preferably, the low speed host

> processor port is internally connected to a **16** bit bus interface connection that provides connection between the protocol analyzer and deep memory trace board. As will be appreciated by those of skill in the art, the bus interface connection internal to the protocol analyzer advantageously operates very much like the PC ISA bus. Further, the data is read out of the deep trace memory under logic step **76** and subsequently the session is terminated under logic step **78**.
>
> The transfer of data from DRAM to the low speed terminal involves the cooperative operation of software logic as shown in **FIG. 7** and hardware as shown in **FIG. 2**. Specifically, DRAM bank **14** operates 2 cycles (40 ns) later than DRAM bank **16**. Thus, for every read access from bank **16** there will be a corresponding access from bank **14**. The address counter is initialized by the user to point to the first address in DRAM of the data to be transferred. The terminal address register is initialized by the user to point to the last address in DRAM to be transferred. Once the data transfer on process is activated, data is read out of the DRAM and stored in a **36** bit register. Only one **36** bit word of the dual bank access is used, the other word is discarded. A second dual bank access is done when the next **36** bits of data is needed.

Applicant respectfully submits that the cited text neither teaches nor suggests "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible," as recited in Applicant's exemplary claim 1. Applicant respectfully submits that, in the Examiner's cited text, the rates across the links of *Bucher* are equal. Applicant respectfully urges that alternating between two transmitting media at equal rates, facilitated by a delay, does not suggest "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible,"

Further, Applicant respectfully submits that nothing in the remaining text of *Bucher* teaches or suggests "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible," as recited in Applicant's exemplary claim 1. Applicant has examined the text of *Bucher* and can find no reference to unequal fractional distribution. Specifically, the words 'numerator', 'fraction' and 'irreducible' are absent from *Bucher*. Applicant respectfully submits that the combination of *Bucher* and *Jou* does not teach or suggest "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one

of said fractions being irreducible," because no combination of the features present in the references would yield Applicant's claimed features.

In addition to failing to teach or suggest, "wherein at least two of said plurality of data rates are unequal and are fractions of said initial rate, all said fractions being capable of reduction to a common denominator and at least one of said fractions being irreducible," the combination of *Bucher* and *Jou* fails to disclose Applicant's controller. The Examiner correctly identifies at page 3 of the present Office Action that "*Bucher* does not explicitly disclose: Controller for controlling said memory and said interfaces and for monitoring a data rate of said data between said memory and said plurality of links, wherein said controller includes means for cyclically distributing data to be communicated from said memory to said second device among said low-peed interfaces, such that each of said plurality of said low speed interfaces receives a number of consecutive units of said data equal to a numerator of its associated fraction." The Examiner then asserts that "in an analogous art, *Jou* discloses a control processor selecting a format that is capable to transmitting data at a selected rate (column 5, lines 35-40, column 8, lines 11-55)." Applicants' amended Claim 1 specifically recites, "wherein said controller includes means for cyclically distributing data to be communicated from said memory to said second device among said low-speed interfaces, such that each of said plurality of low speed interfaces receives a number of consecutive units of said data equal to the numerator of its associated fraction". The cited text of *Jou* discloses at column 8, lines 11-55:

> In the preferred embodiment of the invention, the number of Walsh channels allocated for the high-rate data can be any value 2.sup.N where N32 {2, 3, 4, 5, 6}. The Walsh codes used by Walsh coders **66a-66c** are 64/2.sub.N symbols long, rather than the 64 symbols used with the IS-95 Walsh codes. In order for the high-rate channel to be orthogonal to the other code channels with 64-symbol Walsh codes, 2.sup.N of the possible 64 quaternary-phase channels with 64-symbol Walsh are eliminated from use. Table I provides a list of the possible Walsh codes for each value of N and the corresponding sets of allocated 64-symbol Walsh codes.
>
> *[TABLE I omitted]*
>
> The + and - indicate a positive or negative integer value, where the preferred integer is 1. As is apparent, the number of Walsh symbols in each Walsh code varies as N varies, and in all instances is less than the number of symbols in the IS-95 Walsh channel codes. Regardless of the length of the Walsh code, in the described embodiment of the invention the symbols are applied at a rate of 1.2288 Megachips per second (Mcps). Thus, shorter length Walsh codes are repeated

> more often. Control processor **50** provides a signal to Walsh coding elements **66a-66c** which indicates the Walsh sequence to be used to spread the data.

Similarly the cited text of *Jou* discloses at column 5, lines 11-55:

> After having selected the data rate to be transmitted on each of the carriers, control processor 50 selects a modulation format that is capable of transmitting data at the selected rate. In the exemplary embodiment, different length Walsh sequences are used to modulate the data depending on the rate of the data to be transmitted. The use of different length Walsh sequences selected to modulate the data depending on the rate of the data to be transmitted is described in detail in U.S. Pat. No. 5,930,230, filed May 28, 1996, entitled "HIGH RATE DATA WIRELESS COMMUNICATION SYSTEM", which is assigned to the assignee of the present invention and incorporated by reference herein. In an alternative embodiment, the high rate data can be supported by bundling of CDMA channels as described in the aforementioned U.S. Pat. Nos. 6,005,855 and 5,777,990.

Nothing in the cited text of *Jou* discloses or suggests fractional distribution, the use of irreducible fractions with a common denominator or distribution in proportion to a numerator. Neither *Bucher,* nor the proposed combination of *Bucher* with *Jou* teaches or suggests the combination of elements recited in amended Claim 1.

Given the above reasons, it is clear that the proposed combination of references does not suggest key features of Applicants' claimed invention. Applicants respectfully submit that one skilled in the art would not find Applicants' claimed invention obvious over the combination of references and that the above claims are therefore allowable over the cited combination of references.

II. **No specific teaching of a motivation to combine is cited with respect to Claim 1.**

As set forth in MPEP 2143, the first criterion for establishing a *prima facie* case of obviousness is that "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to...combine reference teachings." In evaluating motivation or suggestion to combine reference teachings, "a prior art reference must be considered in its entirety, *i.e.*, as a whole" (emphasis in original). MPEP 2141.02, citing *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir 1983) *cert. denied*, 469 U.S. 851 (1984). In view of the teachings of the references as taken as a whole, it is apparent that there is no objective suggestion or

motivation in the cited references (or generally in the art) that would lead a skilled artisan to combine the reference teachings to obtain the present invention. If such suggestion or motivation existed, the Examiner would have, no doubt, cited by column and line number a passage in one of the references cited or a well known teaching in the art to discharge his duty to "explain why the combination of the teachings is proper." MPEP 2142, citing *Ex parte Skinner*, 2 USPQ2d 1788 (Bd. Pat. Appl & Inter. 1986). Instead, at page 5 of the present office action, the Examiner asserts:

> Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate or implement Jou's controller in Bucher's device in order to transmit data at a particular rate.

Applicant respectfully disagrees that one skilled in the art would be motivated to combine the references to create Applicant's invention, both because no objective motivation to combine is provided by the cited references and because the cited combination would not result in Applicant's invention. Because the Examiner's combination of references is not supported by any citation to objective teaching in the references or art, Applicant believes that the examiner has failed to establish a *prima facie* case of obviousness.

III. **Arguments with respect to Claim 1 apply broadly**

Applicant respectfully submits that the rejection of exemplary Claim 1 under 35 U.S.C. § 103 is overcome. The foregoing arguments made with respect to Claim 1 are also made with respect to Claims 7 and 10-14, which further limit and patentably distinguish Claim 1. The foregoing arguments are also made with respect to Claims 15-27, which claim a method and a computer program product for performing Applicant's invention, respectively.

CONCLUSION

Applicants have diligently responded to the Office Action to overcome the §103 rejections, and also provided arguments, which show why Applicant's claims are not obvious in light of the references provided. Because the responses and arguments overcome the § 103 rejections, Applicant respectfully requests issuance of a Notice of Allowance for all claims now pending.

Applicant further respectfully requests the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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